CERTIFICATE OF VERIFICATION

I, Su Hyun LEE of 648-23 Yeoksam-dong, Kangnam-ku, Seoul, Korea state that the attached document is a true and complete translation to the best of my knowledge of the Korean-English language and that the writings contained in the following pages are correct English translations of the specifications and claims of the Korean Patent Application Nos. P1997-34196 and P1997-36569.

Dated this 16th day of February, 2004

Signature of translator: ____________

Su Hyun LEE

(Translation)

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[Title of Device] IN-PLANE SWITCHING MODE LIQUID CRYSTAL DISPLAY DEVICE

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[SPECIFICATION]

[TITLE OF THE INVENTION]

IN-PLANE SWITCHING MODE LIQUID CRYSTAL DISPLAY DEVICE

[BRIEF DESCRIPTION OF THE DRAWINGS]

FIG. 1 illustrates an in-plane switching (IPS) mode liquid crystal display device according to the related art.

FIG. 2 illustrates a plan view showing an in-plane switching mode liquid crystal display device according to the first embodiment of the present invention.

FIG. 3(a) illustrates a cross-sectional view taken along line B-B' of FIG. 2.

FIG. 3(b) illustrates a cross-sectional view taken along line C-C' of FIG. 2.

FIG. 4 illustrates an optical axis direction according to the first embodiment of the present invention.

FIG. 5 illustrates driving of liquid crystal molecules according to the first embodiment of the present invention.

FIG. 6 illustrates a liquid crystal panel according to the present invention.

FIG. 7 illustrates an in-plane switching mode liquid crystal display device according to the present invention.

FIG. 8(a) illustrates a plan view showing an in-plane switching mode liquid crystal display device according to the second embodiment of the present invention.

FIG. 8(b) illustrates a cross-sectional view taken along line D-D' of FIG. 8(a).

FIG. 9 illustrates an optical axis direction according to the second embodiment of the present invention.

FIG. 10 illustrates driving of liquid crystal molecules according to the first and

second embodiments of the present invention.

FIG. 11 illustrates the third embodiment of the present invention.

Description of reference numerals for main parts in the drawings

101, 201, 301: gate line	102, 202, 302: data line
103, 203, 303: common line	105, 205, 305: gate electrode
106, 206, 306: source electrode	107, 207, 307: drain electrode
108, 208, 308: data electrode	109, 209, 309: common electrode
110: first substrate	111: second substrate
112: gate insulating layer	115: active layer
116: n^+ layer	123: alignment layer
125, 225, 325: hole	128: black mask
130: liquid crystal layer	132, 133: liquid crystal molecule
135: polarizing plate	136: analyzing plate
139: liquid crystal panel	140: display part
145: frame	147: backlight housing
148: backlight	149: light-guiding plate
150: gate driving circuit	151: gate pad
154: data driving circuit	155: data pad
157: common pad	165: external ground circuit
167: static electricity prevention circuit	

[DETAILED DESCRIPTION OF THE INVENTION]

[OBJECT OF THE INVENTION]

[FIELD OF THE INVENTION AND DISCUSSION OF THE RELATED ART]

The present invention relates to a liquid crystal display (LCD) device, and more particularly, to an in-plane switching (IPS) mode liquid crystal display device having improved aperture ratio and picture quality.

Recently, according as the thin film transistor liquid crystal display devices (TFT-LCDs) have been used as display devices in such applications as portable televisions and notebook computers, it is strongly required to obtain large-sized TFT-LCDs. However, the TFT-LCDs have the problem in that the contrast ratio is changed according to change of viewing angle. In order to solve this problem, twisted nematic LCDs having, for example, optical compensation plates and multi-domains, have been introduced. In these LCDs, however, the color of the image is shifted because the contrast ratio depends on the viewing angle direction.

For a wide viewing angle, the in-plane switching mode LCD is disclosed, for example, in JAPAN DISPLAY 92 P547, Japanese Patent Unexamined Publication No. 7-36058, Japanese Patent Unexamined Publication No. 7-225538, and ASIA DISPLAY 95 P107.

FIG. 1 illustrates an in-plane switching (IPS) mode liquid crystal display device according to the related art. As shown in FIG. 1(a), the in-plane switching mode liquid crystal display device according to the related art includes gate and data lines 1 and 2 formed on a first substrate 10 to define a pixel region, a common line 3 arranged in the pixel region for being in parallel to the gate line 1, a thin film transistor formed at a crossing point of the gate and data lines 1 and 2, and data and common electrodes 8 and 9 formed in the pixel region for being in parallel to the data line 2. As shown in FIG. 1(b), the thin film transistor includes a gate electrode 5 formed on the first substrate 10

for being in contact with the gate line 1, a gate insulating layer 12 deposited on the gate electrode 5, an active layer 15 formed on the gate insulating layer 12, a n^+ layer 16 formed on the active layer 15, and source and drain electrodes 6 and 7 formed on the n^+ layer 16 for being in contact with the data line 2 and the data electrode 8. The common electrode 9 in the pixel region is formed on the first substrate 10 for being in contact with the common line 3, and the data electrode 8 is formed on the gate insulating layer 12 for being in contact with the drain electrode 7 of the thin film transistor. Then, a passivation layer 20 is formed on the thin film transistor, the data electrode 8 and the gate insulating layer 12, and a first alignment layer 23a is deposited thereon to determine alignment direction.

On the second substrate 11, a black matrix layer 28 is formed to prevent leakage of light through the regions of the thin film transistor, the gate line 1, the data line 2, and the common line 3. Then, a color filter layer 29 and a second alignment layer 23b are formed thereon. Also, a liquid crystal layer 30 is formed between the first and second substrates 10 and 11.

In the aforementioned in-plane switching mode LCD device, an electric field being in parallel to the first and second substrates 10 and 11 is generated between the data and common electrodes 8 and 9 when a voltage is applied from an external driving circuit. Accordingly, liquid crystal molecules aligned in the liquid crystal layer 30 are rotated according the electric field, thereby controlling the amount of light passing through the liquid crystal layer 30.

However, the in-plane switching mode LCD device according to the related art has the following disadvantages.

First, since the data and common electrodes 8 and 9 are formed of opaque metal,

the aperture ratio is lowered.

Second, the passivation layer 20 is deposited on the data electrode 8, and the gate insulating layer 12 and the passivation layer 20 are formed on the common electrode 9, whereby the electric field applied in the liquid crystal layer 30 is absorbed to the gate insulating layer 12 and the passivation layer 20, whereby the intensity of the electric field applied to the liquid crystal layer 30 is decreased. Thus, driving speed of the liquid crystal molecules is decreased so that the image may be disconnected during obtaining moving picture.

Third, the gate and data lines 1 and 2 should be apart from the pixel region so as to avoid the crosstalk problem due to the electric field generated by the gate and data lines 1 and 2, thereby lowering the aperture ratio.

[TECHNICAL TASKS TO BE ACHIEVED BY THE INVENTION]

An object of the present invention is to provide an in-plane switching (IPS) mode LCD device, in which the aperture ratio is improved by increasing the actual pixel region in a method of partially overlapping a common electrode with gate and data lines.

Another object of the present invention is to provide an in-plane switching (IPS) mode LCD device to improve picture quality by slantingly forming a common electrode in a crossing portion of data and common electrodes.

To achieve these and other advantages and in accordance with the purpose of the present invention, as embodied and broadly described, an in-plane switching (IPS) mode LCD device includes first and second substrates, gate and data lines crossing each other on the first substrate to define a pixel region, a thin film transistor at a crossing point of the gate and data lines, a common line formed in the pixel region for being

parallel to the gate line, a data electrode formed in the pixel region for being parallel to the data line, a common electrode formed in parallel to the data electrode for being partially overlapped with the gate and data lines so as to prevent an electric field generated by the gate and data lines, a first alignment layer deposited on an entire surface of the first substrate, a black mask formed on the second substrate, a color filter layer formed on the black mask, a second alignment layer formed on the color filter layer, and a liquid crystal layer formed between the first and second substrates.

At this time, the thin film transistor includes a gate electrode being in contact with the gate line, a gate insulating layer deposited on the entire surface of the first substrate above the gate electrode, an active layer formed on the gate insulating layer, a n^+ layer formed on the semiconductor layer, and source/drain electrodes formed on the n^+ layer.

Also, the data electrode is formed on the gate insulating layer for being in contact with the source/drain electrodes, and the common electrode of transparent ITO is formed on a passivation layer for being in contact with the common line through a hole. The data and common electrodes form a storage capacity therebetween, whereby it is possible to apply the dual storage capacity to the LCD device.

At a crossing portion of the data and common electrodes, the common electrode is formed at the slanting structure. Thus, the liquid crystal molecules near to the crossing portion are rotated at the same direction as those of the middle region of the pixel region. Preferably, the slanting direction of the common electrode is about 45° on the gate line.

[PREFERRED EMBODIMENTS OF THE INVENTION]

Hereinafter, an in-plane switching mode liquid crystal display (IPS-LCD) device according to the present invention will be described with reference to the accompanying drawings.

FIG. 2 illustrates an in-plane switching mode LCD device according to the first embodiment of the present invention. As shown in FIG. 2, a plurality of gate and data lines 101 and 102 are formed on a substrate, thereby defining a plurality of pixel regions. In the actual LCD device, 'n' gate lines 101 and 'm' data lines 102 are formed on the substrate so as to define '$n \times m$' pixel regions. For reference, one pixel region will be descried in the accompanying drawings. In the pixel region, a common line 103 is formed parallel to the gate line 101, and a thin film transistor is formed at a crossing point of the gate and data lines 101 and 102. Also, data and common electrodes 108 and 109 formed in the pixel region are arranged in parallel to the data line 102. At this time, the data and common electrodes 108 and 109 are formed on the common line 103. The common electrode is in contact with the common line 103 through a hole 125 of a passivation layer. Also, as shown in the drawings, the common electrode 109 is partially overlapped with the gate and data lines 101 and 102. By overlapping of the common electrode 109, it is possible to avoid the crosstalk since the common electrode 109 prevents an electric field generated by the gate and data lines 101 and 102.

FIG. 3(a) illustrates a cross-sectional view taken along line B-B' of FIG. 2. As shown in FIG. 3(a), the thin film transistor includes a gate electrode 105 formed on a first substrate 110, a gate insulating layer 112 deposited on the gate electrode 105, an active layer 115 formed on the gate insulating layer 112, a n^+ layer formed on the active layer 115, and source and drain electrodes 106 and 107 formed on the n^+ layer. At this time, the gate electrode 105 is simultaneously formed with the gate line 101 and the

common line 103, which is formed by etching dual metal layers of Mo/Al layers, the Al layer having a thickness of 2000Å and the Mo layer having a thickness of 1000Å deposited by sputtering. Also, the gate insulating layer 112 is formed by depositing an inorganic material such as SiNx on the first substrate 110 at a thickness of 4000Å in a chemical vapor deposition (CVD) method. The active layer 115 and n^+ layer 116 are respectively formed by etching an amorphous silicon (a-Si) having a thickness of 1700Å and a n^+ a-Si layer having a thickness of 300Å in the CVD method. The data line 102, the source electrode 106, the drain electrode 107 and the data electrode 108 are formed by etching Cr layer having a thickness of 1500Å. As shown in FIG. 2, the gate electrode 105 of the thin film transistor is connected with the gate line 101, the source electrode 106 is connected with the data line 102, and the drain electrode 107 is connected with the data electrode 108.

On the thin film transistor, the gate line 108 and the gate insulating layer 112, the passivation layer 120 of SiNx having a thickness of 2000Å is deposited, and then the common electrode 109 is formed thereon. The common electrode 109 is a transparent conductive layer of ITO (indium tin oxide) deposited at a thickness of 500Å by sputtering, wherein the common electrode 109 is partially overlapped with the drain electrode 107.

A first alignment layer 123a is deposited on the common electrode 109 and the passivation layer 120. In case of that the alignment layer 123a is formed of polyimide, an alignment direction thereof is determined by mechanical rubbing. In case of the alignment layer is formed of photo-reactive materials such as PVCN (polyvinylcinnamate) or polysiloxane based materials, an alignment direction thereof is

determined by irradiation of ultraviolet light. In the light-alignment process, the alignment direction of the alignment layer is determined according to the polarizing state, the polarizing direction and the number of light irradiation. Generally, if the polysiloxane or PVCN based materials are used for the alignment layer, the alignment direction is determined by irradiating the ultraviolet light at one or two times. In the method of irradiating the light at one time, it is possible to irradiate non-polarized light, polarized light (especially, linearly polarized light), or partially polarized light to be slant on the alignment layer. In the method of irradiating the light at two times, it is possible to irradiate polarized light to be slant on or vertical to the alignment layer at one time, after determining the two alignment directions of degeneracy, the polarized light is irradiated again, whereby the desired alignment direction is selected.

As shown in FIG. 2, a hole 125 is formed in the passivation layer 120, whereby the common electrode 109 is in contact with the common line 103 through the hole 125. FIG. 3(b) illustrates a cross-sectional view taken along line C-C' of FIG. 2, which shows the contact of the common line 103 and the common electrode 109 by the hole 125. As shown in the drawings, the data electrode 108 and the common electrode 109 are respectively connected with metal lines formed on the gate insulating layer 112 and the passivation layer 120. In this case, the metal lines are formed of the same metal material as the data electrode 108 and the common electrode 109. Accordingly, the gate insulating layer 112 and the passivation layer 120 are respectively deposited between the common line 103 and the metal line being in contact with the data electrode 108, and between the metal line being in contact with the common electrode 109 and the metal line being in contact with the data electrode 108. That is, as shown in the drawings, a total storage capacity Cst of the present invention is formed of the sum of

first and second storage capacities Cst1 and Cst2, the first storage capacity Cst1 between the data electrode 108 and the common electrode 109, and the second storage capacity Cst2 between the common line 103 and the data electrode 108. Thus, the total storage capacity Cst of the present invention is greater than that of the related art. At this time, the common electrode 109 is partially overlapped with the data line 120, whereby it is possible to prevent the crosstalk by the data line 102.

On a second substrate 111, a black mask 128 as a black matix layer and a color filter layer 129 are formed. At this time, it is possible to form an overcoat layer on the black mask 128 and the color filter layer 129 so as to obtain stability and improve flatness on a surface of the second substrate 111. The black mask 128 prevents a leakage of light through the regions of the gate line 101, the data line 102, the common line 103 and the thin film transistor. The black mask 128 is formed of Cr/CrOx layer or black resin having a thickness of 1㎛ and a width of 10㎛ in each region. In the color filter layer 129, one of R, G and B layers are repetitively formed in each pixel region. After depositing the second alignment layer 123b of polyimide or photo-reactive material on the color filter layer 129, the alignment direction is determined by rubbing or light irradiation. Also, liquid crystal is injected between the first and second substrates 110 and 111 in a vacuum state, thereby forming a liquid crystal layer 130.

FIG. 4 illustrates driving of liquid crystal molecules according to the first embodiment of the present invention, and FIG. 5 illustrates an optical axis direction. In the drawings, θ_{EL}, θ_R and θ_E respectively indicates the extension direction of the data electrode 108 and the common electrode 109, an alignment direction of the alignment layer, and an electric field direction between the data and common electrodes

108 and 109. As shown in the drawings, the data electrode 108 and the common electrode 109 are formed in parallel to the extension direction of the data line 102 (θ_{EL}=90°). Also, the alignment direction determined in the alignment layer (θ_R) is 0°<θ_R<90°. As shown in FIG. 5, the liquid crystal molecules are aligned according to the alignment direction θ_R. As a voltage is applied to the electrodes, the electric field of θ_E=0° is generated between the data and common electrodes 108 and 109. Thus, the liquid crystal molecules 132 are rotated in the clockwise direction, whereby the liquid crystal molecules 132 are aligned along the electric field direction θ_E. In the drawings, the liquid crystal molecules of spotted line show the liquid crystal molecules when the voltage is not applied, and the liquid crystal molecules of solid line show the liquid crystal molecules when the voltage is applied.

In the in-plane switching mode LCD device having the aforementioned structure, the common electrode 109 formed on the passivation layer 120 is partially overlapped with the gate and data lines 101 and 102, so that it is possible to avoid the crosstalk by preventing the electric field generated by the gate and data lines 101 and 102. As compared with the related art where the gate and data lines 101 and 102 are apart from the pixel region obtaining the actual image at the predetermined distance, the present invention obtains the larger pixel region, thereby improving the aperture ratio.

Also, since the common electrode 109 is formed on the passivation layer 120, it is possible to prevent absorption of the electric field by the insulating layer. Thus, the electric field having the great intensity is applied to the liquid crystal layer 130. In this respect, the driving voltage is lowered. Also, in case of that the common electrode 109 is formed of transparent ITO, the aperture ratio is improved. Furthermore, as shown in

FIG. 3(b), the storage capacity Cst is greatly increased as compared with that of the related art, thereby stabilizing the voltage applied to the liquid crystal layer 130. Also, even though the storage capacity similar to that of the related art is applied, it is possible to improve the aperture ratio since storage capacity region is decreased.

FIG. 6 illustrates a thin film transistor array substrate according to the present invention. As shown in FIG. 6, the respective gate and data lines 101 and 120 crossing each other for defining the pixel region are in contact with the external driving circuit through the gate pad 151 and the data pad 155. Also, the gate line 101 and the data line 102 are in contact with the external ground line 165 through the static electricity prevention circuit 167 formed of the thin film transistor. The static electricity prevention circuit 167 is formed between the gate and data lines 101 and 102. The source and drain electrodes of the static electricity prevention circuit 167 are in contact with the data line 102. Also, the common line 103 is grounded on the external through the common pad 157.

Although not shown, the pad 151, 155, 157 is formed of a plurality of metal layers. At this time, the first metal layer is generally used of Mo/Al layer, and the second metal layer is formed of Cr layer. Generally, the passivation layer 120 deposited in the pixel region is sequentially formed on the pad 151, 155, 157. Accordingly, in order to connect the liquid crystal panel with the external driving circuit, it is required to etch the passivation layer of the pad region. This process for etching the passivation layer is progressed simultaneously when forming the hole 125. However, according as the pad 151, 155, 157 exposed to the external by etching is in contact with the external air, an oxidation layer is formed thereon, thereby increasing contact resistance. In the preferred embodiment of the present invention, when

forming the common electrode 109 of ITO on the passivation layer 120, the ITO is deposited on the pad region, whereby it is possible to prevent the oxidation layer on the surface of the pad.

FIG. 7 illustrates the in-plane switching mode LCD device according to the present invention, wherein FIG. 7(a) illustrates the plan view, and FIG. 7(b) illustrates the cross-sectional view taken along line D-D' of FIG. 7(a). As shown in FIG. 7(a), the gate driving circuit 150 and the data driving circuit 154 are arranged in the inside of an external frame 145 of a display part 140, whereby the gate and data driving circuits 150 and 154 are in contact with the gate and data lines 101 and 102 of the display part 140 through gate and data pads 151 and 155.

As shown in FIG. 6(b), a backlight 148 is provided inside a backlight housing 147 on the external frame 145, whereby light is projected on the liquid crystal panel 139 through a light-guiding plate 149. Then, a polarizing plate 135 is formed between the light-guiding plate 149 and the liquid crystal panel 139 so as to linearly polarize the light, and an analyzing plate 136 is formed outside of the liquid crystal panel 139.

FIG. 8 illustrates the second embodiment of the present invention, and FIG. 9 illustrates the optical axis direction. As shown in the drawings, a common electrode 209 is partially overlapped with gate and data lines 201 and 202, so that it is possible to prevent crosstalk generated by the gate and data lines 201 and 202. In the second preferred embodiment of the present invention, both sides of the common electrode 209 are provided to be slant to a data electrode 208. In the drawings, 'A' and 'B' regions indicate regions showing the slanting structure of the common electrode 209. As shown in FIG. 7, the extension direction θ_{EL} of the electrode 208, 209, the alignment direction θ_R and the electric field direction θ_E are the same as those in the first

embodiment of the present invention. In the 'A' region, the slanting direction θ_A of the common electrode 209 is $\theta_R < \theta_A < \theta_R + 90°$. In the 'B' region, the slanting direction, the slanting direction θ_B is $90° - \theta_R < \theta_B < 180° - \theta_R$.

As shown in the preferred embodiment of the present invention, the common electrode 209 is formed in the slanting structure, whereby it is possible to prevent disclination by the common electrode 209 and the data electrode 208 in the LCD device according to the first embodiment of the present invention as well as the crosstalk by the gate line 201 and the data line 202, thereby improving picture quality in the in-plane switching mode LCD device according to the present invention.

In the electrode structure according to the first embodiment of the present invention, when applying the voltage, the electric field is generated between the electrodes 108 and 109 as shown in FIG. 10(a). That is, in the middle region, the electric field direction θ_E is vertical to the extension direction θ_{EL} of the electrodes 108 and 109. However, in 'A' and 'B' regions of the drawings, the crossing portion of the data electrode 108 and the common electrode 109, the curvelinear electric field is generated between the electrodes 108 and 109 being in vertical. When the voltage is not applied thereto, the liquid crystal molecules 132 are aligned along the alignment direction θ_R. As the voltage is applied thereto, the liquid crystal molecules 132 are rotated and aligned along the electric field direction θ_E. In the middle region as shown in the drawings, the liquid crystal molecules 132 are rotated in the clockwise direction for being in vertical to the extension direction θ_{EL} of the electrodes 108 and 109. In 'A' and 'B' regions of the drawing, since the electric field is generated in the curvelinear form, the liquid crystal molecules 132 are aligned at the different direction

from those of the middle region. The alignment direction of the liquid crystal molecules may be principal causes for generating the disclination problem in the 'A' and 'B' regions. Especially, the liquid crystal molecules 132 of 'A' region are rotated at the opposite direction to those of the middle region and 'B' region, thereby generating serious disclination problem. In the drawings, the disclination indicates as the line having spots, and the disclination causes the problem of lowering the picture quality.

In the second embodiment of the present invention, both sides of the common electrode 209, formed at the crossing portion of the data and common electrodes 208 and 209, have the slanting structure for the data electrode 208. As shown in FIG. 8(b), the liquid crystal molecules 132 of 'A' and 'B' regions are rotated at the same direction as those of the middle region, thereby preventing the disclination in 'A' and 'B' regions.

In the second embodiment of the present invention, the common electrode 209 of transparent metal such as ITO is formed on the passivation layer in the same manner as the first embodiment of the present invention so as to improve the aperture ratio. Also, it is possible to form the dual storage capacity by the common electrode 209 and the data electrode 208.

FIG. 11 illustrates the third embodiment of the present invention. The third embodiment of the present invention has the same structure as the second embodiment of the present invention except slanting directions of electrode. At this time, the slanting directions θ_A, θ_B of the common electrode 309 are θ_A=45° and θ_B=135°, and the alignment direction of alignment layer θ_R is θ_R=75°.

[ADVANTAGES OF THE INVENTION]

As mentioned above, the in-plane switching mode LCD device according to the present invention has the following advantages.

In the in-plane switching mode LCD device according to the present invention, the common electrode is partially overlapped with the gate and data lines. As compared with the related art in-plane switching mode LCD device for obtaining the predetermined distance between the actual pixel region and the gate and data lines so as to avoid the crosstalk by the gate and data lines, the in-plane switching mode LCD device according to the present invention has the improved aperture ratio. Also, when forming the common electrode, the common electrode overlapped with the data line has the slanting structure so that it is possible to prevent the disclination by the electric field between the common electrode and the data line at the crossing portion of the common electrode and the data electrode.